

CLAIMS

- 1 1. A method for shaping a baseband signal comprising:
2 providing a plurality of coefficient memories, each having a plurality of
3 coefficients values representing filter response waveform values;
4 determining a coefficient memory address for each of the coefficient
5 memories;
6 addressing each of the plurality of coefficient memories;
7 retrieving an addressed coefficient value from each of the plurality of
8 coefficient memories;
9 providing a negative value for each of the retrieved ones of the plurality of
10 coefficient values;
11 selecting in response to the baseband signal, one of the retrieved coefficient
12 value and the negative value; and
13 summing the selected value from each coefficient memory for providing a
14 shaped signal.
- 1 2. The method of Claim 1 further comprising sharing the plurality of coefficient
2 memories for shaping both an in-phase baseband signal and a quadrature baseband
3 signal.
- 1 3. The method of Claim 2 wherein sharing the plurality of memories comprises:
2 retrieving one of the coefficient values corresponding to the in-phase
3 baseband signal on a first edge of a clock signal; and
4 retrieving one of the coefficient values corresponding to the the quadrature
5 baseband signal on a different second edge of the clock signal.
- 1 4. The method of Claim 3 wherein the clock signal comprises a digital to analog
2 converter clock signal.
- 1 5. The method of Claim 1 wherein determining a coefficient memory address

2 comprises:

3 determining an increment for providing a predetermined number of samples
4 for each of a plurality of symbols comprising the baseband signal; and
5 incrementing an address counter in response to the predetermined number of
6 samples for each symbol and a predetermined coefficient memory size.

1 6. The method of Claim 1 wherein the baseband signal comprises an in-phase
2 signal and a quadrature signal;

3 wherein selecting the coefficient value comprises selecting an in-phase value
4 in response to the in-phase signal and selecting a quadrature value in response to the
5 quadrature signal; and

6 wherein summing the selected value comprises summing the selected in phase
7 value from each coefficient memory for providing a shaped in phase signal and
8 summing the selected quadrature value from each coefficient memory for providing a
9 shaped quadrature signal.

1 7. The method of Claim 1 wherein the negative value comprises at least one of:
2 a 2's complement value;
3 an offset binary value; and
4 a signed magnitude value.

1 8. The method of Claim 1 wherein providing a plurality of coefficient memories
2 comprises combining at least two filter coefficients for forming the plurality of
3 coefficient values such that coefficient memory storage is minimized.

1 9. The method of Claim 1 further wherein providing a plurality of coefficient
2 memories further comprises providing coefficient memories corresponding to a
3 plurality of roll-off factors.

1 10. The method of Claim 1 wherein the plurality of coefficient memories further
2 includes one of:
3 the sum of a first filter response value and a second filter response value; and
4 the difference of a first filter response value and a second filter response value.

- 1 11. The method of Claim 10 wherein the first filter response and the second filter
2 response are symmetric.
- 1 12. The method of Claim 10 wherein retrieving coefficient values comprises:
2 providing an address counter having a plurality of logic outputs for addressing
3 the coefficient memories; and
4 determining whether to retrieve one of the sum and the difference in response
5 to selected ones of the logic outputs.
- 1 13. The method of Claim 12 further comprising:
2 providing a logic circuit having an output, a first input coupled to a logic
3 output of the address counter, a second input coupled to an in-phase data symbol bit
4 and a third input coupled to a quadrature data symbol bit;
5 determining whether to select one of the retrieved value and the negative value
6 in response to the output of the logic circuit.
- 1 14. The method of Claim 10 wherein summing the selected value comprises:
2 providing a plurality of adder stages, each adder coupled to a pipeline register;
3 clocking the pipeline register at a digital to analog converter (D/A) rate; and
4 scaling and formatting the summed values after a final adder stage.
- 1 15. The method of Claim 10 wherein the baseband signal is clocked at a symbol
2 rate and the retrieval of coefficients is clocked at a digital to analog converter (D/A)
3 rate such that the number of retrievals per coefficient equals the D/A rate divided by
4 the symbol rate.
- 1 16. The method of Claim 10 wherein the filter waveform comprises a raised
2 cosine.
- 1 17. The method of Claim 10 wherein the filter waveform comprises a square root
2 raised cosine.
- 1 18. A method for shaping a baseband signal comprising:
2 providing a plurality of digital words, each digital word indicating a

3 coefficient value at an instant of time;
4 selecting responsive to the baseband signal, one of the digital words and a
5 corresponding negative value of the digital word; and
6 summing the selected digital word for providing a baseband shaped signal.

1 19. The method of Claim 18 wherein providing a plurality of digital words
2 comprises combining at least two filter coefficients for forming the plurality of
3 coefficient values such that coefficient memory storage is minimized.

1 20. A device comprising:
2 a plurality of coefficient memories, each memory having an input address bus,
3 a multiplexor input and a coefficient value output;
4 a plurality of first registers, each having an input coupled to a respective one
5 of the coefficient value outputs, a digital to analog (D/A) clock input and an output;
6 a plurality of negative value circuits, each circuit having an input coupled to a
7 respective one of the first register outputs, and an output;
8 a plurality of 2:1 multiplexors, each having a first input coupled to a respective
9 one of the first register outputs and having a second input coupled to a respective one
10 of the output of the plurality of negative value circuits ;
11 a plurality of second registers, each having an input coupled to a respective
12 one of the outputs of the plurality of 2:1 multiplexors, a digital to analog (D/A) clock
13 input and an output; and
14 an adder having a plurality of inputs coupled to respective ones of the plurality
15 of second registers.

1 21. The device of Claim 20 wherein each of the plurality of negative value circuits
2 comprises at least one of:
3 a 2's complement logic element;
4 an offset binary logic element; and
5 a signed magnitude logic element.

1 22. The device of Claim 20 further comprising a coefficient address generator
2 having an output coupled to a coefficient memory input address bus, the input address
3 having a plurality of address lines.

1 23. The device of Claim 22 wherein the coefficient address generator further
2 comprises:
3 an adder having a plurality of address output lines;
4 an address register coupled to the plurality of address output lines and having
5 clocked address line outputs and an address counter most significant bit output;
6 an exclusive or logic gate (XOR) array having address inputs coupled to the
7 clocked address lines outputs and an address counter most significant bit input
8 coupled to the address counter most significant bit output, and outputs coupled to a
9 corresponding plurality of the plurality of address lines of the coefficient memory
10 address bus; and
11 an XOR multiplexor having inputs coupled a pair of baseband bit signals
12 and an output coupled to one of the plurality of address lines of the coefficient
13 memory address bus.